

We claim:

1. A method for forming MOS transistor gate dielectrics,
comprising:

5 providing a semiconductor substrate;

 forming a first dielectric layer on said semiconductor
substrate;

10 performing a first plasma nitridation of said first
dielectric layer;

 removing said first dielectric from a region of said
substrate;

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 forming a second dielectric layer on said semiconductor
substrate in said region from which said first dielectric layer
were removed; and

20 simultaneously performing a second plasma nitridation of
said second dielectric layer and said first dielectric layer.

2. The method of claim 1 wherein said first dielectric layer
comprises silicon oxide.

3. The method of claim 2 wherein said second dielectric layer comprises silicon oxide.

5 4. The method of claim 1 wherein said second dielectric layer has a final nitrogen concentration of 5 to 15 atomic percent following said first and second plasma nitridation.

10 5. The method of claim 4 wherein said first dielectric layer has a nitrogen concentration of 5 to 20 atomic percent following said second plasma nitridation.

6. A method for forming integrated circuit MOS transistors,
comprising:

providing a semiconductor substrate;

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forming a first silicon oxide layer;

performing a plasma nitridation process on said first
silicon oxide layer forming a first plasma nitrided oxide layer;

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removing said first plasma nitrided oxide layer from
regions of said substrate;

forming a second plasma nitrided oxide layer on said
semiconductor substrate in said regions from which said first
plasma nitrided oxide layer was removed.

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7. The method of claim 6 wherein said forming said second plasma
nitrided oxide layer comprises:

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forming a second silicon oxide layer in said regions from
which said first plasma nitrided oxide layer was removed; and

performing a second plasma nitridation process on said second oxide layer and said first plasma nitrided oxide layer.

- 5 8. The method of claim 7 wherein said first plasma nitrided oxide layer comprises 5 to 15 atomic percent of nitrogen.

9. Integrated circuit MOS transistors, comprising:

a semiconductor substrate;

5 a first plasma nitrided oxide layer formed on a first region of said semiconductor substrate;

a second plasma nitrided oxide layer formed on a second region of said semiconductor substrate wherein said second
10 plasma nitrided oxide layer is formed using dual nitridation processes;

a first transistor gate formed on said first plasma nitrided oxide layer; and

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a second transistor gate formed on said second plasma nitrided oxide layer.

10. The integrated circuit MOS transistors of claim 9 where said
20 first plasma nitrided oxide layer comprises 5 to 20 atomic percent of nitrogen.

11. The integrated circuit MOS transistors of claim 10 where said second plasma nitrided oxide layer comprises 5 to 15 atomic percent of nitrogen.